

# Fully Depleted, Monolithic Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias

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## Abstract

A new pixel design using pinned photodiode (PPD) in a 180 nm CMOS image sensor (CIS) process has been developed as a proof of principle. The sensor can be fully depleted by means of reverse bias applied to the substrate, and the principle of operation is applicable to very thick sensitive volumes. Additional n-type implants under the in-pixel p-wells have been added to the manufacturing process in order to eliminate the large parasitic substrate current that would otherwise be present in a normal device. The new design exhibits nearly identical electro-optical performance under reverse bias as the reference PPD pixel it is based on, and the leakage current is effectively suppressed. The characterisation results from both front- and back-side illuminated sensor variants show that the epitaxial layer is fully depleted.

## Introduction

Silicon pinned photodiode (PPD) sensors are widely used today in high performance imaging due to their low readout noise, high conversion gain and low dark current. For applications requiring high quantum efficiency (QE) in the near-infrared and soft X-ray bands, the active sensor depth should reach tens or even hundreds of micrometres. Thick sensitive semiconductor volumes are depleted by applying reverse bias across the substrate, so that field-free regions are eliminated and the photogenerated charge is promptly collected. The magnitude of the reverse bias depends on the resistivity and the thickness of the semiconductor substrate and can far exceed any other voltage in the system.

Presently this is achievable with hybrid CIS or CCDs, but is a challenge for monolithic PPD devices. PPD CIS are active pixel sensors which contain at least 3 transistors in a p-well next to the PPD, as shown in Figure 1. The front side p-wells are at the sensor's substrate potential and are connected to ground. Applying negative substrate bias  $V_{BSB}$  at the back of the device in order to increase the depletion depth under the PPD would result in large currents flowing from the front side p-wells to the backside  $p^{++}$  contact, as the  $p^+/p^-/p^{++}$  structure conducts resistively. Eliminating this parasitic current would allow the full substrate thickness to be depleted, and is the main objective of this development.

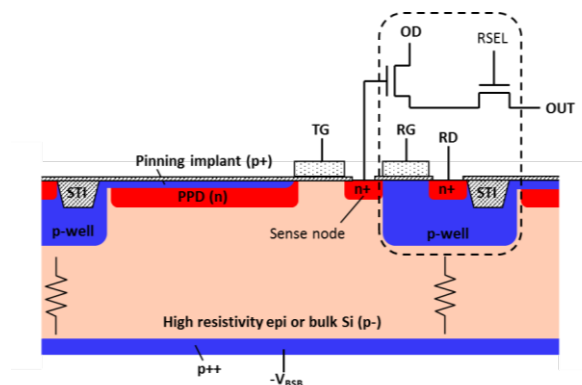


Figure 1 – Cross section of a typical PPD pixel. The source follower and the select transistor are physically situated in the in-pixel p-well.

## Pixel and Sensor Design

The new pixel design implements a deep, lightly doped n-type implant under the in-pixel p-wells, as shown in Figure 2. This implant, called “deep depletion extension” (DDE) is floating and does not connect to the PPDs [1][2].

In normal operation the DDE acquires its potential from the adjacent PPDs and becomes depleted. By choosing the appropriate doping profile and size of the DDE, its potential can be made lower than the pinning voltage  $V_{pin}$ , but still high enough to create a potential barrier. The DDE region acts as a bridge extending the depletions from the PPDs underneath the p-wells, creating a pinch-off and a potential barrier of sufficient height to prevent undesired substrate currents.

The first prototype chip, called BSB1, was designed by the CEI and manufactured on 1000  $\Omega\cdot\text{cm}$ , 18  $\mu\text{m}$  epitaxial wafers using the well-established 180 nm CMOS image sensor process from TowerJazz Semiconductor. BSB1 includes four image arrays each of 10  $\mu\text{m}$  and 5.4  $\mu\text{m}$  pixel pitch with different size of the DDE implant and also three doping profiles – shallow, medium and deep. A simplified cross section, showing the most important elements in the design is shown in Figure 2.

Subsequently, some wafers were processed by e2v Technologies for backside illumination (BSI), using their proprietary back-thinning process. The final epitaxial thickness of the BSI chip variant has been reduced from 18  $\mu\text{m}$  to 12  $\mu\text{m}$ . A photograph of the two chip variants is shown in Figure 3.

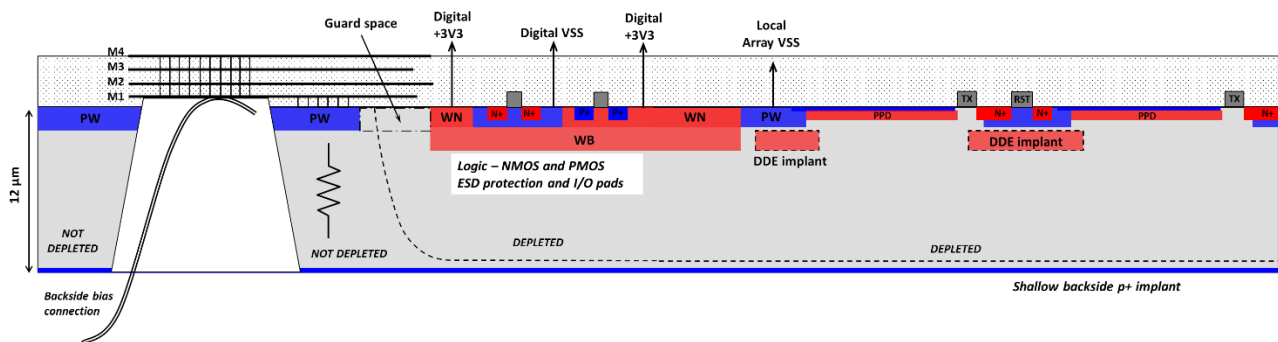


Figure 2 – Simplified cross section of the new sensor.

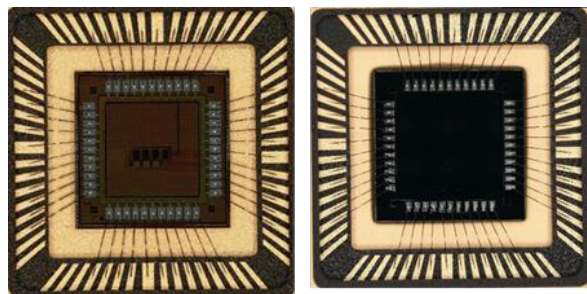


Figure 3 – Photographs of the FSI (left) and the BSI (right) BSB1 chip variants.

## Characterisation results

The measurements show that all chip variants can be reverse biased without significant leakage currents, and that this is maintained under strong illumination [3]. At sufficiently high reverse voltages the potential barrier created by the DDE is reduced, and leakage current caused by thermionic emission of holes begins to flow. The onset of this is beyond full depletion, and the voltage threshold depends on the size and depth of the DDE as predicted by TCAD simulations.

Most of the new pixel variants exhibit nearly identical electro-optical performance to the reference, as shown in the photon transfer curves (PTC) in Figure 4. The PTC is an important characterisation tool which allows the measurement of the conversion gain of the device, readout noise and full well capacity, and is sensitive

to subtle effects in pixel operation, such as charge re-distribution, which demonstrate as irregularities in the PTC.

The measured conversion gain for the 10  $\mu\text{m}$  and 5.4  $\mu\text{m}$  pixels was 78  $\mu\text{V}/\text{e}^-$  and 38  $\mu\text{V}/\text{e}^-$  respectively, and it is close to the design values. The shape of the PTC and the conversion gain do not change under reverse bias, which indicates that the new DDE implant does not interfere with the normal pixel operation and charge transfer. There was no difference in the response between the FSI and BSI devices.

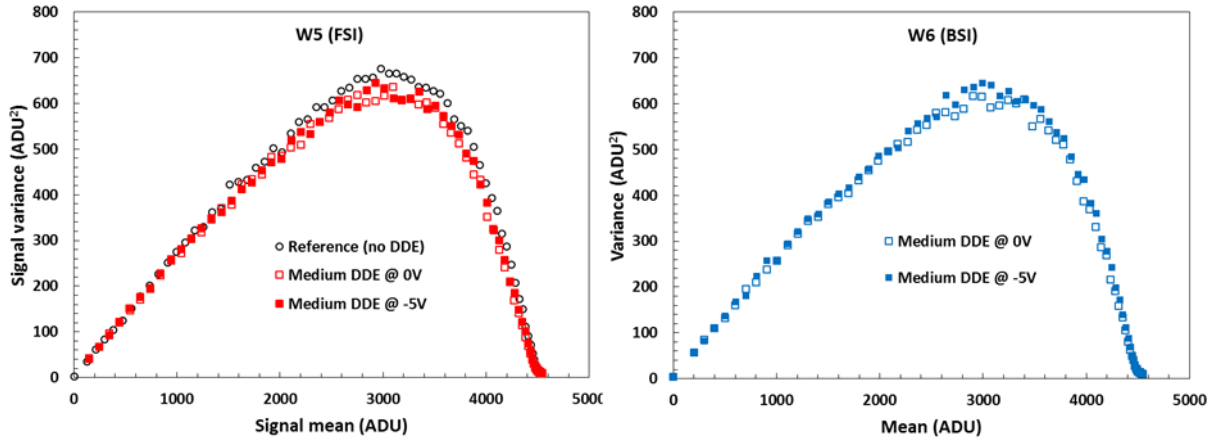


Figure 4 – Photon transfer curves of a 10  $\mu\text{m}$  pixel in a FSI chip (left) and a BSI chip (right).

Dark current measurements were used in FSI devices to estimate the onset of full depletion due to the nearly full suppression of the surface dark current, which leaves the bulk dark as dominant. As the depletion increases in depth it reaches the backside interface with the  $\text{p}^{++}$  substrate and cannot increase anymore; at this point the bulk dark current is expected to level off. Figure 5 shows the measured dark current in two pixel array variants as a function of the backside bias. The data is consistent with the expectation of full depletion at -4V reverse bias, and the observed dark current is typical for the technology.

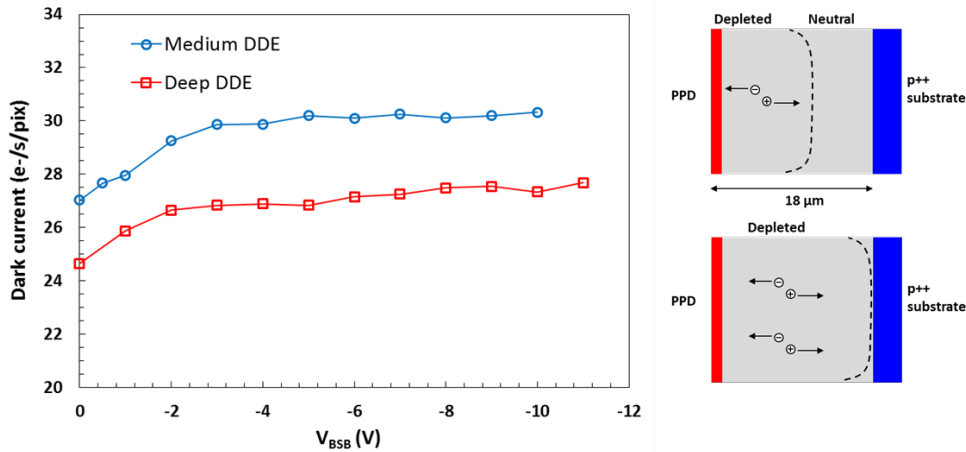


Figure 5 – Dark current in a 10  $\mu\text{m}$  pixel in a FSI device under reverse bias, and a diagram illustrating the measurement principle.

In BSI devices the dark current is a factor of 5 higher than in FSI devices at room temperature due to traps at the back surface, which are not fully neutralised by the passivating  $\text{p}^{++}$  backside implant, and this method cannot be used. Spot illumination was used as an additional technique to confirm that the depletion reaches the back surface in BSI devices. To avoid the use of optics, which adds uncertainty, a precision pinhole on a thin steel foil was placed in contact with the device surface. Short wavelengths (for example 470 nm, 0.6  $\mu\text{m}$  absorption length in silicon) are absorbed near the backside, and if that region is field-free the charge will diffuse somewhat before being collected. However, if the depletion reaches the back of the device there will be less diffusion, and the projected spot will appear sharper. Much longer wavelengths (for example 940 nm,

54  $\mu\text{m}$  absorption length) are absorbed throughout the thickness of the device and the charge spread is much less sensitive to the extent of depletion, in particular in our relatively thin 12  $\mu\text{m}$  BSI devices.

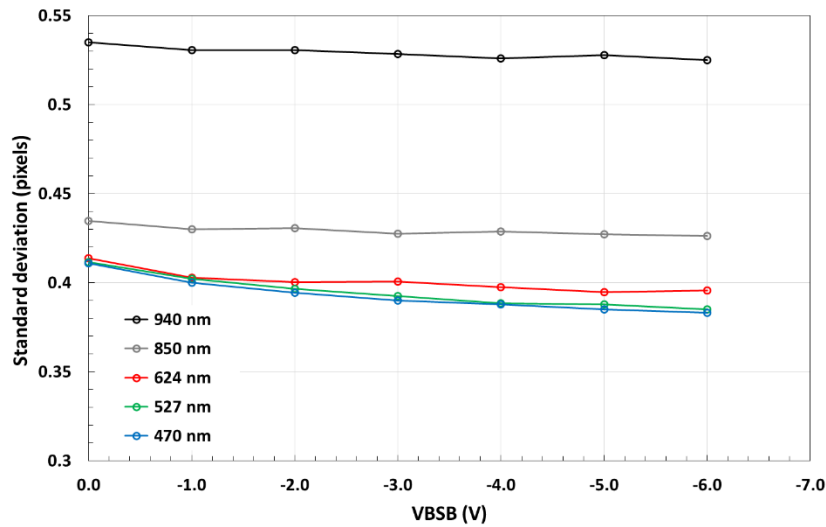


Figure 6 – Standard definition of the Gaussian fit for a 10  $\mu\text{m}$  pinhole spot projection for on a 10  $\mu\text{m}$  pixel array in a BSI chip under reverse bias.

From the decrease of the spot size with increasing reverse voltage, shown in Figure 6 for shorter wavelengths, we can conclude that the depleted region does increase with the reverse voltage. This effect is a lot less prominent for near-IR light, as theorised above.

## Conclusions

The work presented in this paper has demonstrated a new operating principle of reverse biasing of monolithic PPD image sensors in order to increase their sensitive volume and QE. The new pixel design can be reverse biased beyond full depletion, and demonstrated that the leakage currents can be suppressed in good agreement with TCAD simulations. The leakage mechanism is based on thermionic emission of holes and is inherent to the operation principles of the device, however this occurs beyond full depletion and is not a limitation. The leakage from the peripheral logic, off-pixel circuitry and the specially designed ESD protection pads is negligible. The depletion depth has been confirmed using dark current and spot light illumination methods.

This development has the potential to greatly increase the quantum efficiency of PPD CIS at near-infrared and soft X-ray wavelengths, as the operating principle allows sensors with sensitive volumes in excess of 100  $\mu\text{m}$  to be fully depleted.

## References

- [1] K.D. Stefanov, “CMOS Image Sensor with Backside Biased Substrate”, patent application GB1404363.2; US 2015/0263058 A1; EP 2 919 270 A1.
- [2] K.D. Stefanov, A.S. Clarke and A.D. Holland, “Fully Depleted and Backside Biased Monolithic CMOS Image Sensor”, in Proc. SPIE 9915, 991513, (2016), doi: 10.1117/12.2232413.
- [3] K.D. Stefanov, A.S. Clarke and A.D. Holland, “Fully Depleted Pinned Photodiode CMOS Image Sensor With Reverse Substrate Bias”, IEEE Electron Device Letters, Vol. 38, No. 1, pp. 64-66 (2017), doi: 10.1109/LED.2016.2625745.